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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,093	08/31/2000	Randhir P.S. Thakur	94-0302.02	5663

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,093	THAKUR ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. In view of the Appeal Brief filed on July 12, 2002, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

This office action is submitted to correct a minor technical error in typing the Office Action dated February 1, 2002. It should be noted that only figures 4 – 6 are relied upon with reference to Doan. The issue of inherency has been removed because the dielectric layer of Doan is a TEOS layer which is used by the applicant to form the disclosed dielectric layer.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. The term "generally" in claim 60 is a relative term which renders the claim indefinite. The term "generally" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is not clear how insulative, conductive or laterally coextensive anything preceded by the term "generally" is in this claim (i.e. "generally insulative material", "generally conductive element", "generally laterally coextensive"). Does generally laterally coextensive mean that the generally conductive element is laterally coextensive for the entire length of the generally insulative material, or is the generally conductive element only laterally coextensive with a portion of the length of the generally insulative material.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doan et al. (USPAT 5372974, Doan) in view of Boland et al. (USPAT 5084407, Boland).

Doan discloses a method of processing a semiconductor device in figure 6.

With regard to claim 52, Doan discloses in figure 6 depositing a dielectric layer (50) over a semiconductor substrate. Doan discloses in figure 6 and column 4, lines 28 – 44 allowing electrically chargeable particles to occur in the dielectric layer, because the dielectric layer is tetraethylorthosilicate ("TEOS"). Doan discloses in figure 6 and column 4, lines 28 – 44 allowing some diffusion of the electrically chargeable particles, because the dielectric layer is

TEOS. Doan discloses in figure 6 and column 4, lines 17 – 20 preventing at least some of the electrically chargeable particles from reaching the substrate, because of the silicon nitride barrier layer (40). Doan does not disclose that the substrate comprises a plurality of electrically conductive regions and an electrically insulative region therebetween. Boland discloses in figure 2 a substrate that comprises a plurality of electrically conductive regions (22) and an electrically insulative region (12) therebetween. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the substrate of Boland in the method of Doan in order to provide a planar surface of isolated areas and active areas that allow semiconductor devices to be smaller, denser and have a larger number of layers that are vertically stacked as stated in the abstract and column 1, lines 9 – 29 of Boland.

6. Claims 53 – 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan in view of Cunningham et al. (USPAT 5468689, Cunningham).

With regard to claim 53, Doan discloses in figure 6 and column 4, lines 28 – 44 depositing a dielectric layer (50) over a semiconductor substrate, wherein the step of depositing a dielectric layer of TEOS comprises depositing a dielectric layer using an organic precursor. Doan discloses in figure 6 and column 4, lines 28 – 44 allowing electrically chargeable particles to occur in the dielectric layer, wherein the step of allowing electrically chargeable particles to occur in the dielectric layer comprises allowing an organic component of the organic precursor to deposit in the dielectric layer, because the dielectric layer is TEOS. Doan discloses in figure 6 and column 4, lines 28 – 44 wherein a feature at the molecular level is allowing some diffusion of the electrically chargeable particles, because the dielectric layer is TEOS. Doan discloses in

figure 6, column 3, lines 60 – 68 and column 4, lines 1 – 44 preventing at least some of the electrically chargeable particles from reaching the substrate, wherein the preventing step comprises layering a barrier of silicon nitride (40) over the substrate using plasma processing prior to the step of depositing a dielectric layer. Doan is silent in teaching that the plasma-processing step used to deposit the barrier uses a non-organic precursor. Cunningham teaches in the abstract depositing a layer of silicon nitride using a non-organic precursor in a plasma process. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the non-organic precursor process of Cunningham in the method of Doan in order to form a barrier layer that can withstand oxide desorption at temperatures in excess of 900 degrees Centigrade as taught by Cunningham in column 1, lines 44 – 45.

With regard to claim 54, Cunningham discloses in the abstract that the plasma processing layering step comprises layering a barrier using silane.

With regard to claim 55, Doan discloses in figures 4 – 6 a method of at least partially forming a circuit device. Doan discloses in figures 4 – 6 providing a semiconductor substrate (30). Doan discloses in figures 4 – 6 layering a barrier (40) on the substrate. Doan discloses layering a carbon-containing dielectric layer on the barrier, because the dielectric is TEOS. Doan does not disclose that the barrier is carbon-free. Cunningham teaches a method of layering a carbon-free barrier on a substrate in the abstract. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the carbon-free barrier method of Cunningham in the method of Doan in order to form a barrier layer that can withstand oxide desorption at temperatures in excess of 900 degrees Centigrade as taught by Cunningham in column 1, lines 44 – 45.

With regard to claim 56, Cunningham discloses in the abstract that the step of layering a carbon-free barrier on the substrate further comprises layering the carbon-free barrier using a plasma.

With regard to claim 57, Doan discloses further comprising a step of heating the carbon-containing dielectric in column 4, lines 44 and 45.

7. Claims 58 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Cunningham as applied to claims 55 – 57 above, and further in view of Ying (USPAT 5384288).

With regard to claim 58, Doan and Cunningham is silent to the teaching the step of heating the carbon-containing dielectric comprises raising a temperature to a range of 850C – 1050C for at least 5 seconds. Ying teaches in column 4, lines 18 – 22 the step of heating a carbon-containing dielectric comprising raising a temperature to a range of 850C – 1050C for at least 5 seconds. While Ying teaches a few seconds and not directly at least 5 seconds it would be apparent to the skilled artisan that at least 5 seconds in the rapid thermal anneal environment of Ying would result in a sufficient anneal. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the rapid thermal anneal of Ying in the method of Doan and Cunningham in order to reflow the carbon containing dielectric layer with a process using a low reflow temperature that has less of a probability of damaging the circuit beneath as stated by Ying in column 4, lines 18 – 33.

With regard to claim 59, Doan and Cunningham do not directly disclose the step of heating the carbon-containing dielectric comprises raising a temperature to a range of a range of 750C-1000C for at least 5 minutes. Ying teaches in column 4, lines 18 – 22 the step of heating a

carbon-containing dielectric comprising raising a temperature to a range of 750C-1000C for at least 5 minutes. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the steam ambient anneal of Ying in the method of Doan and Cunningham in order to reflow the carbon containing dielectric layer with a process using a low reflow temperature that has less of a probability of damaging the circuit beneath as stated by Ying in column 4, lines 18 – 33.

8. Claims 60, 61, 63 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan in view of Ghezzi et al. (USPAT 5132239, Ghezzi).

With regard to claim 60, Doan discloses a method of processing a substrate in figures 4 – 6. Doan discloses in figure 5 depositing an oxide charge barrier over the substrate (silicon nitride). Doan discloses in figure 6 depositing a generally insulative material (TEOS) over the oxide charge barrier, wherein the generally insulative material is less insulative that the barrier. Doan does not disclose a substrate comprising two active areas and an intervening insulating region, and providing a generally conductive element. Ghezzi teaches in figure 3 a substrate (2) comprising two active areas and an intervening insulating region and providing a generally conductive element (5) over a generally insulative material (21), wherein the element is generally laterally coextensive with the intervening insulating region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the active areas and generally conductive element of Ghezzi in the process of Doan in order to form a floating gate for an EEPROM memory cell which will have several advantages over older technology both in

efficiency and reliability as stated by Ghezzi in column 1, lines 40 – 46, column 3, lines 31 – 40 and 55 – 56 and column 4, lines 1 – 27.

With regard to claim 61, Doan discloses in column 4, line 43 the step of depositing a generally insulative material comprises depositing a generally insulative material that is allowed to comprise oxide charges.

With regard to claim 63, Doan discloses in figure 6 and column 4, lines 44 and 45 annealing the generally insulative material. Doan discloses in figure 6 and column 4, lines 44 and 45 allowing an oxide charge in the generally insulative material to migrate toward the substrate in response to the annealing step, because the generally insulative material is TEOS. Doan discloses in figure 6 and column 4, lines 17 – 20 intercepting the oxide charge with the oxide charge barrier before the oxide charge reaches the substrate, because the oxide charge barrier is silicon nitride.

With regard to claim 64, Doan discloses in figure 6 refraining from depositing any generally conductive material before the step of depositing a generally insulative material.

9. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Ghezzi as applied to claim 60 above, and further in view of Van Der Scheer et al. (USPAT 4976856, Van Der Scheer)

Doan and Ghezzi are silent in the teaching plasma treating the substrate. Van Der Scheer teaches in column 1, lines 28 – 32 plasma treating a substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the plasma treating method of Van Der Scheer to treat the substrate in the method of Doan and Ghezzi in order for

the preparation of non-porous (i.e. dense) membrane layers that have a much higher ability to allow select transport of molecular species as stated by Van Der Scheer in column 3, lines 8 – 20.

Response to Arguments

10. Applicant's arguments filed July 12, 2002 have been fully considered but they are not persuasive.

With regard to the applicant's arguments regarding claim 52, the applicant has not fully addressed the rejection as strongly suggested in the explanation of the rejection.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
August 15, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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